IN THE CLAIMS:

1. (Currently amended) A clock alignment circuit comprising:

an input for receiving a first clock signal;

an input for receiving a second clock signal having a period N times that of the first clock signal, N being an integer greater than or equal to two;

an output for outputting a third clock signal also having a period N times that of the first clock signal;

phase comparison means for providing an indication of whether the closest edge of a particular kind of the first clock signal to an edge of a particular kind of the second clock signal is earlier or later than that edge, the [[said]] kinds of edges being positive going or negative going and the [[said]] ones of the first and second clock signals being of the same kind or of different kinds; and

third clock signal providing means, for providing the third clock signal from the second clock signal, comprising latching means, for latching the second clock signal, operable to latch and delay the second clock signal by such an amount, dependent on the [[said]] indication from the phase comparison means, that the resulting third clock signal has an edge, either positive or negative going, aligned with the [[said]] closest edge of the first clock signal.

2. (Currently amended) A clock alignment circuit as claimed in claim 1, wherein the latching means comprises a first latch responsive to the first clock signal to latch the second clock signal, or a delayed version thereof, on a particular kind of edge of the first clock signal, and a second latch responsive to the first clock signal to latch the second clock signal, or a delayed version thereof, on the other kind of edge of the first clock signal, the third clock signal providing means being arranged to use the output of the first latch in the provision of the third clock signal if said indication from the phase comparison means is that the [[said]] edge is late and to use the output of the second latch if it is early.

3. A circuit as claimed in claim 2 comprising a multiplexer responsive to said indication to select between the outputs of the first and second latches or delayed versions thereof.

4. A circuit as claimed in claim 2 wherein the latching means comprises at least one further latch connected to latch, and thereby delay, the output of the first or second latch at times defined by the first clock signal.

5. A circuit as claimed in claim 2 wherein the latching means comprises at least one further latch connected to latch, and thereby delay, the second clock signal, or a delayed version thereof, at times defined by a fourth clock signal, and to pass that delayed second clock signal to the first and second latches, the fourth clock signal having a period of 1/M times that of the second clock signal and having edges aligned with said particular kind of edge of the second clock signal.

6. A circuit as claimed in claim 5 wherein N=M.

7. (Currently amended) A circuit as claimed in claim 1, wherein the latching means provides a version of the second clock signal to the first and second latches so delayed that an edge of that version of the second clock signal falls substantially at a position at an interval equal to one period of the first clock signal before the [[said]] edge of said particular kind of the second clock signal.

8. (Currently amended) A circuit as claimed in claim 5, wherein the phase comparison means is responsive to the phases of the first clock signal and [[a, or the,]] the fourth clock signal having a period of 1/M times that of the second clock signal and having edges aligned with said particular kind of edge of the second clock signal, to produce said indication.

9. A circuit as claimed in claim 1 wherein the third clock signal providing means comprises as oscillator for generating the third clock signal, and phase adjustment means is responsive to the delayed second clock signal provided by the latching means to adjust the phase of the third clock signal generated by the oscillator.

10. A circuit as claimed in claim 9 wherein the oscillator comprises a counter.

11. A circuit as claimed in claim 9 wherein the phase adjustment means comprises an edge detector connected to detect an edge of a particular kind in the delayed second clock signal provided by the latching means.

12. (Currently amended) A circuit for adjusting the phase of a plurality of word clocks for a respective plurality of data streams having a respective plurality of bit clocks, the bit clocks each having edges aligned with the bits of the respective data stream and the word clocks each having a period that is an integer multiple of that of the respective bit clock,

the circuit comprising a plurality of phase adjustment circuits, each for so producing the word clock for a respective one of the data streams in response to a word clock for another one of the data streams and the bit clock for its own data stream that the word clock produced has an edge of a particular kind aligned with the edge of a particular kind of the bit clock for its own data stream that is closest to an edge of a particular kind of the word clock for the [[said]] other data stream,

wherein one of the data streams is a master data stream and the circuit comprises means for producing the word clock for that data stream from its bit clock without reference to the phase of the word clocks of the other data streams.

13. A circuit as claimed in claim 12, wherein at least some of the phase adjustment circuits are connected in daisy-chain fashion with the first of those connected to receive the word clock for the master data stream and subsequent ones being connected to receive the word clock from the previous one.

14. A circuit as claimed in claim 12 wherein two or more of the phase adjustment circuits are connected to receive the word clock for the master data stream.

15. (Currently amended) A circuit as claimed in claim 12, wherein each phase adjustment circuit is [[a clock adjustment circuit as claimed in any one of claims 1 to 11 each]] connected so that the first clock signal is the bit clock signal for the data stream of that phase adjustment circuit, the second clock signal is the word clock signal for said other data stream and the third clock signal is said word clock signal for the data stream of that phase adjustment circuit.

16. (Currently amended) A method of aligning a second clock signal to a first clock signal, the second clock signal having a period N times that of the first clock signal, N being an integer greater than or equal to two, to provide a third clock signal also having a period N times that of the first clock signal, the method comprising:

providing an indication of whether the closest edge of a particular kind of the first clock signal to an edge of a particular kind of the second clock signal is earlier or later than that edge, the [[said]] kinds of edges being positive going or negative going and the [[said]] ones of the first and second clock signals being of the same kind or of different kinds; and

providing the third clock signal from the second clock signal, that providing comprising latching, and thereby delaying, the second clock signal by such an amount, dependent on the [[said]] indication that the resulting third clock signal has an edge, either positive or negative going, aligned with the [[said]] closest edge of the first clock signal.

17. (Currently amended) A method as claimed in claim 16, wherein the latching comprises latching the second clock signal, or a delayed version thereof, in response to the first clock signal on a particular kind of edge of the first clock signal and latching the second clock signal, or a delayed version thereof, in response to the first clock signal on the other kind of edge of the first clock signal, wherein the one of those latched versions

of second clock signal that is used in the providing of the third clock signal is selected in response to said indication of whether the [[said]] edge is late or early.

18. A method as claimed in claim 16 wherein the latching further comprises latching, and thereby delaying, the second clock signal, or a delayed version thereof, at times defined by a fourth clock signal, and passing that delayed second clock signal to be the version of the second clock signal latched on both kinds of edge of the first clock signal, the fourth clock signal having a period of 1/M times that of the second clock signal and having edges aligned with said particular kind of edge of the second clock signal.

19. A method as claimed in claim 18 wherein N=M.

20. (Currently amended) A method as claimed in claim 17, wherein the latching provides such a version of the second clock signal for the latching on both kinds of edge of the first clock signal that an edge of that version of the second clock signal falls substantially at a position at an interval equal to one period of the first clock signal before the [[said]] edge of said particular kind of the second clock signal.

21. (Currently amended) A method as claimed in claim 16, wherein the [[said]] indication is provided in response to the first clock signal and a, or the, fourth clock signal having a period of 1/M times that of the second clock signal and having edges aligned with said particular kind of edge of the second clock signal.

22. A method as claimed in claim 16 wherein the providing of the third clock signal comprises generating the third clock signal with an oscillator, and adjusting the phase of the third clock signal so provided in response to the delayed second clock signal provided by the latching.

23. A method in claim 22 wherein the adjusting comprises edge detecting an edge of a particular kind in the delayed second clock signal provided by the latching.

24. (Currently amended) A method adjusting the phase of a plurality of word clocks for a respective plurality of data streams having a respective plurality of bit clocks, the bit clocks each having edges aligned with the bits of the respective data stream and the word clocks each having a period that is an integer multiple of that of the respective bit clock,

the method comprising using a plurality of phase adjustment circuits, each for so producing the word clock for a respective one of the data streams in response to a word clock for another one of the data streams and the bit clock for its own data stream that the word clock produced has an edge of a particular kind aligned with the edge of a particular kind of the bit clock for its own data stream that is closest to an edge of a particular kind of the word clock for the [[said]] other data stream,

wherein one of the data streams is a master data stream and the circuit comprises means for producing the word clock for that data stream from its bit clock without reference to the phase of the word clocks of the other data streams.

25. A method as claimed in claim 24, wherein at least some of the phase adjustment circuits are connected in daisy-chain fashion with the first of those connected to receive the word clock for the master data stream and subsequent ones being connected to receive the word clock from the previous one.

26. A circuit as claimed in claim 24 wherein two or more of the phase adjustment circuits are connected to receive the word clock for the master data stream.

27. (Currently amended) A method as claimed in claim 24, wherein each phase adjustment circuit is [[a clock adjustment circuit as claimed in any one of claims 61 to 68 each]] connected so that the first clock signal is the bit clock signal for the data stream of that phase adjustment circuit, the second clock signal is the word clock signal for said other data stream and the third clock signal is said word clock signal for the data stream of that phase adjustment circuit.